Micheal E. Cater II

181 Cummings Rd.
Thorndale, TX. 76577

Home: (512) 434-2329 Cell: (515)289-8602
email: rocket7@farm-market.net

SUMMARY

Organized, self-motivated, creative problem-solver with experience in Systems Design and Development, and Hardware Applications Engineering. Expertise in designs from concept to production, high speed digital interfaces and FPGA design. Works well in a team or as an individual contributor

Technical Aptitudes

Viewdraw/DxDesigner	**Mentor Graphics DA**	**Orcad (Design Entry CIS)**	**Concept (Design Entry HDL)**
Allegro PCB Editor	**Constraint Manager**	**HDL Designer**	**ModelSim**
Precision Synthesis	**Altera Quartus II**	**MAXPLUS II**	**Lattice ispLEVER**
Xilinx ISE	**Verilog**	**Novas Debussy**	**FrameMaker**
Word	**Excel**	**PowerPoint**	**Visio**
PCI Express	**Serial Rapid I/O**	**Gigabit Ethernet**	**DDR, DDR2 and DDR3**
SRAM	**PCI**	**Flash**	**I2C, SPI and UART**
Oscilloscope	**Logic analyzer**	**UNIX**	**C, C++ and assembly**

PROFESSIONAL EXPERIENCE

Freescale Semiconductor, Austin, TX 2004 – Present

Senior Hardware Engineer

Designed test cards, reference cards and development systems for new PowerQUICC III processors. Designed entire system, entered schematics, entered electrical and routing constraints, directed layout and routing of the PCB, bring-up and debug of the design and support of the design with both internal and external customers. Designed and implemented several Interposers boards to allow for initial board bring-up before the initial silicon for the new processor was in house. Designs included PCI Express (Gen 1 and Gen 2) and Serial Rapid IO (SRIO) for high speed serial interfaces, DDR2/3 memory, local bus sections, multiple Giga-bit Ethernet ports, power-on reset support, I2C and SPI interfaces and UART support.

Provided review of customer design based on PowerQUICC III processors including schematic and layout. Developed and gave presentations to FAEs and customers along with application and design notes.

Designed and coded FPGA for new Data path control card. Designed several High-Speed Bridge card to connect two test cards together and allow for testing of multiple PCI Express interfaces.

Volt, Inc. (Contract with **AMD**), Austin, TX 2004 – 2004

Electrical Engineer

Tested and verified customer designs using AMD processors including the Athlon and Opteron. Tests included HyperTransport and DDR interfaces.

Intrinsity, Inc., Austin, TX 2002 – 2004

Hardware Application Engineer

Provided hardware applications engineering for the company. Provided support for the 2GHz FastMATH and FastMIPS processors. Wrote and updated applications notes, customer and new employee training on these parts and support of the evaluation/development board. Designed the latest revision of the FastMATH evaluation board and updated the documentation for the design.

Designed FPGA to translate a RapidIO port to a PCI Bus interface. Designed test board for this FPGA, using DxDesigner for schematic entry and will work with a local layout house for the PCB design and manufacturing.

Aerotek, Inc. (Contract with **General Dynamics Land Systems**), Tallahassee, FL 2002 – 2002

Electrical Design Engineer

Designed a VME64x backplane for the upgrade of the M1A2 Mission Processor Unit. The backplane included interfaces to USB, Firewire, Fibre Channel, Ethernet (10BaseT and 100BaseTX), serial ports and 1553 utility bus. This included schematic entry (DxDesigner and DxAnalog), writing documentation for the project (Microsoft Office), working with CAD on board layout and design verification.

IBM, Austin, TX 2000 - 2001

Advisory Engineer

Provided customer support as a Hardware Applications Engineering for the 750CX/CXe PowerPC microprocessor. Answered customer design questions, maintained customer specific and general specifications, wrote application notes and validation test plans including schedules for validation.

Cisco Systems, Inc., Austin, TX 1999 - 2000

Hardware Engineer

Re-designed Network Interface card for Cisco DSLAMs. This included schematic entry (Viewlogic), component selection, writing hardware functional specifications (FrameMaker and Microsoft Office) and design verification testing. Re-design for worldwide use of the Quad CAP/DMT line card. This included schematic entry, component selection, writing hardware functional specifications and design verification testing. This project is now in production. Prior to this I did the final re-spin of the 2 port CAP line card. This project saw limited production and was replaced by the 4 port card. I also work on providing BERT (Bit Error Rate Testing) capability for the 2 port DMT line card. Experience with various chipsets involving Mixed-signal design.

Cisco Systems, Inc., San Jose, Ca 1996 - 1999

Hardware Engineer

Design and development of an ATM based ADSL DMT, issue 2 modem. This included schematic entry, PLD design and testing to interface to the motherboard and debug of the design. The PLD was done with Altera AHDL and the MaxPlus II software. Schematic entry was done with Viewlogic. The project was in hardware verification and performance testing at time of transfer to Austin. Experienced with various chipsets involving Mixed-signal design.

Design and development of an ISDN-U interface router, the 1604. This included schematic entry, debug and testing to the ANSI T1.601 specification in the lab and at Bellcore. This project took 6 months from start of the System Functional Specification to FCS (First Customer Shipment). There was also the redesign of the 1604 to improve performance and solve problems that arose form the interactions of different Central Office switch types and the MLT (Metallic Loop Termination) circuit. Required several trips to customer sites to gather data and re-testing the fixed units at these sites. The final revision included a Run-From-RAM feature.

Other projects included design of an SDSL WIC (WAN Interface Card) for the 1600 and other platforms, including PLD design, schematic entry and layout. Took initial schematics for the Micro Web Server from an outside consultant and converted to Cisco standards before the project went to CAD group for layout, including development of symbols for the schematics.

Integrated Device Technology, Santa Clara, Ca. 1992 - 1996

Senior Hardware Application Engineer

Senior Applications Engineer in the RISC Microprocessor Group. Became the group expert for the all 64-bit CPUs including the R4600, R4700, R4000/4400, R4650 and the R5000. Also support all 32-bit CPU and support chips for both the 64 and 32-bit processors. Designed evaluation board for the R4600 and R4650 and designed a module which plugs into the CPU socket for the R5000 with an on board secondary cache. All design projects done with Viewlogic schematic entry tools and netlisters and Altera FPGAs for all system controllers. Ran Verilog simulations of the R4600, R4700, R4650 and R5000 CPUs to help answer customer and internal questions about the architecture and normal operations.

Taught and developed several sections of the RISC training class, wrote specifications for new products, provided customer support on the RISC Hotline and design review of customer designs and wrote technical users manuals and applications, technical notes and conference papers on the various processors and their use (using FrameMaker and Microsoft Office including PowerPoint). Developed code in C, C++ and MIPS assembly to help solve problems for customers and for internal test development.

LSI Logic, Milpitas, Ca. 1989 - 1992

Hardware Application Engineer

Applications Engineer in the MIPS Microprocessor group. Provided support for 32-bit, R3000 based CPU module, the LR33000 32-bit CPU and the 64-bit, MIPS R4000. Supported 16-bit military 1750A CPU and MMU and development of a CPU core for ASICs based on the L64500 CPU.

Education

MS, Electrical Engineering, Stanford University, Stanford, Ca.

BS, Computer Engineering, University Of Illinois, Urbana, IL.